TFT LCD Approval Specification

MODEL NO.: N121X4-L02

Customer: Dell Computer Corporation

Approved by: _____

Note:

Liquid Crystal Display Division	
QRA Division.	OA Head Division.
Approval	Approval
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REVISION HISTORY

Date	Document Revision	Page	Summary
March 24, 2004	OEM I-N121X4-L02	All	First Edition for customer.
July 7, 2004	OEM I-N121X4-L02-02		Second edition
Oct. 6, 2004	OEM I-N121X4-L02-03	Page 6 Page 11	2.1Product Summary: fixed typo: Storage temp –20 to 60degC 6Optical Characteristics: Color chromaticity changed
Oct. 25, 2004	OEM I-N121X4-L02-04	Page 10	5Mechanical Characteristics: mounting hole position 2.8mm -> 2.5mm
Nov.11, 2004	CAS-I-N121X4-L02-D01	Page 13 Page 28 Page 21 Page 33 Page 35 Page 37	Added 6.2 Luminance Uniformity Added 7.7BIST Added 7.4EEDID Added 9Qualifications and CFL Life Added 10Packaging Added 11Labels
Dec. 6, 2004	CAS-I-N121X4-L02-D02	Page 4 Page 6 Page 11 Page 11 Page 20 Page 21 Page 27 Page 30 Page 31 Page 31 Page 32 Page 39	1 Handling Precautions: UL 1950 => UL 60950 Table 1 Product summary: B/L power consumption 4.6W max => 4.4W max 6.1 Optical Characteristics: Viewing angle 40 typ => 40 min, etc. 6.1 Optical Characteristics: White luminance 120 min => 127 min 7.3.1 Timing Characteristics: changed V-total time min 777 => 780 7.4 EEDID: Revision X02 data 7.6 Power ON/OFF Sequence: VESA style symbols 8.1 Interface Connector: Added description of LAMP_STAT pin Table 19 Electrical Specifications: Input power changed(4.6W max=-> 4.4W max), P(5VSUS) 25mW max => 70mW max, P(5VALW) 10mW max => 10mW max 8.2 Electrical Characteristics: Removed dimming table Figure 16 SMData – Luminance: Updated. 12 Appendix Fixed typo: UL 60960 => UL 90950, SELF => SELV
Mar. 8, 2005	CAS-I-N121X4-L02-D03	Page 7 Page 10 Page 21 Page 30 Page 36	2.2 Functional Block Diagram: Added BISTEN to block diagram 5 Mechanical Characteristics: Corrected label position in reference drawing 7.4 EEDID: Corrected BIST Enable Flag(7Ah) 0 => 1 8.1 Interface Connector: Corrected part number(lead-free type) 10 Packaging Specifications: Added packaging type (B)
May. 16, 2005	CAS-I-N121X4-L02-D04	Page 38	11.3 PPID Label; Corrected REV code (A00 => A02)

1. Handling Precautions

- If any signals or power lines deviate from the power on/off sequence, it may cause shorten the life of the LCD module.
- The LCD panel and the CFL are made of glass and may break or crack if dropped on a hard surface, so please handle them with care.
- CMOS ICs are included in the LCD panel. They should be handled with care, to prevent electrostatic discharge.
- Do not press the reflector sheet at the LCD module to any directions.
- Do not stick the adhesive tape on the reflector sheet at the back of the LCD module.
- Please handle with care when mount in the system cover. Mechanical damage for lamp cable/lamp connector may cause safety problems.
- Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (2.11, IEC60950 or UL60950), or be applied exemption conditions of flammability requirements (4.4.3.3, IEC60950 or UL60950) in an end product.
- The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit (2.4, IEC60950 or UL60950).
- The fluorescent lamp in the liquid crystal display (LCD) contains mercury. Do not put it in trash that is disposed of in landfills. Dispose of it as required by local ordinances or regulations.
- Never apply detergent or other liquid directly to the screen.
- Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
- When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth; do not use solvents or abrasives.
- Do not touch the front screen surface in your system, even bezel.
- Gently wipe the covers and the screen with a soft cloth.

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2. General Description

- This specification applies to 12.1 inch Color TFT/LCD Module 'N121X4-L02'.
- This module is designed for a display unit of notebook style personal computer.
- The screen format and electrical interface are intended to support the XGA (1024(H) x768 (V)) screen.
- This module contains an inverter card for backlight.
- BIST (Built-In Self Test) function
- VESA CVT reduced blanking mode support
- Compliant with RoHS (Restriction of the Use of Certain Hazardous Substances) directive

2.1 Product Summary

Table 1 shows the summary of this LCD module. Unless otherwise noted, all characteristics are at 25 degree C condition.

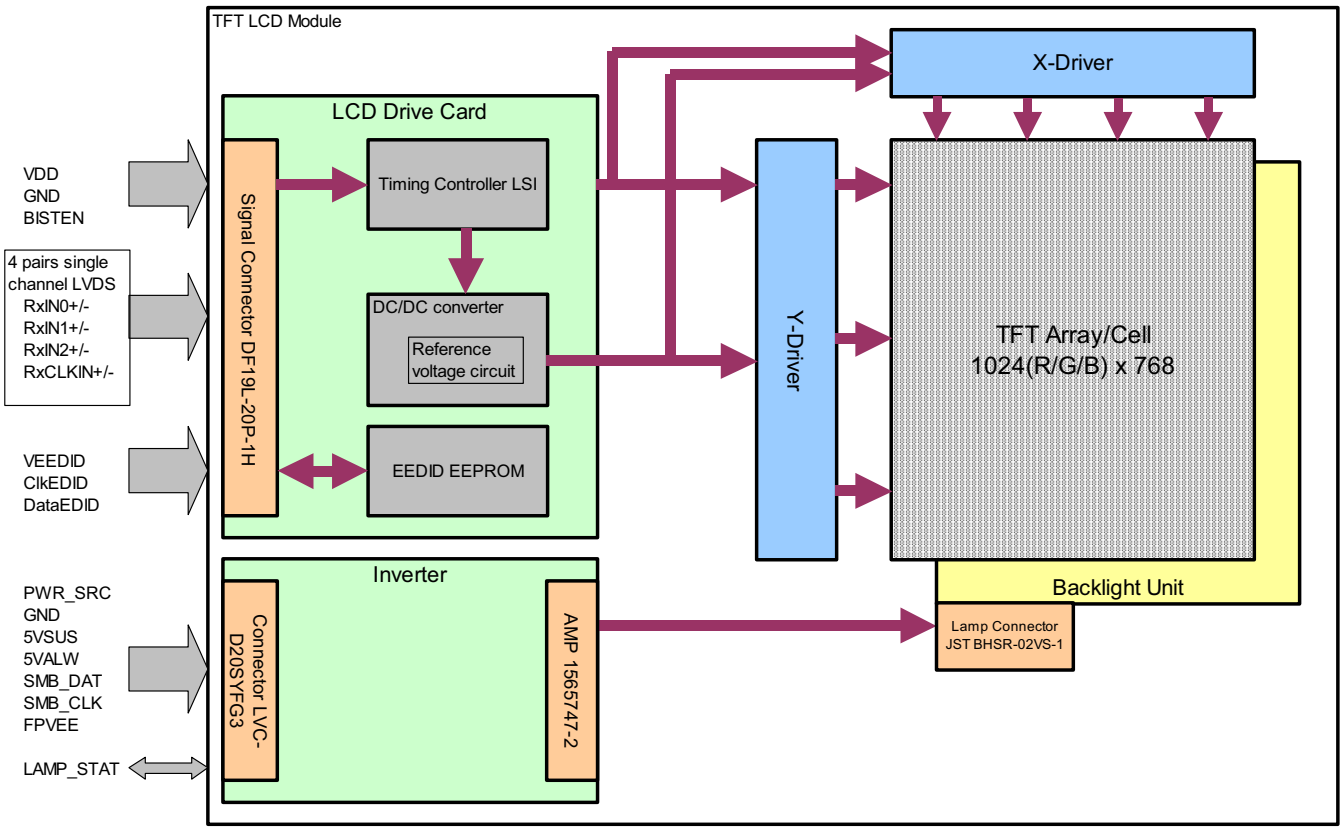
Table 1 Product summary

ITEMS	SPECIFICATIONS
Screen Diagonal [mm]	307.2
Active Area [mm]	245.76(H) x 184.32(V)
Pixels H x V	1024(x3) x 768
Pixel Pitch [mm]	0.240(per one triad) x 0.240
Pixel Arrangement	R.G.B. Vertical Stripe
Display Mode	Normally White
White Luminance [cd/m2]	150 typ. (5 Points average, SMData=00H)
Contrast Ratio	300: 1 Typ.
Optical Rise Time + Fall Time [msec]	50Max.
Nominal Input Voltage[Volt] VDD 5VSUS, 5VALW line PWR_SRC line	 +3.3 Typ +5.0 Typ +14.4 Typ.
Logic Power Consumption [watt](VDD Line)	0.9 Typ. (All Black Pattern)
Backlight Power Consumption [watt]	4.4 Max(SMData=00H)
Weight [grams]	280 Typ, 295 max. (with inverter)
Physical Size [mm]	261.0(W) x 209.5(H) x 4.7(D) Typ. (with Inverter space) 261.0(W) x 198.0(H) x 4.7(D) Typ. (without inverter space)
Electrical Interface (Logic)	Single LVDS(4 pairs LVDS) EEDID (clock, data) BISTEN
Electrical Interface (Inverter)	SMB_CLK, SMB_DAT, FPVEE, LAMP_STAT
Support Color	Native 262K colors (RGB 6-bit data driver)
Temperature Range (degree C) Operating Storage (Shipping)	 0 to +50 -20 to +60

2.2 Functional Block Diagram

Figure 1 shows the functional block of the color TFT/LCD Module:

Figure 1 Block Diagram



3. Absolute Maximum Ratings

Table 2 Absolute maximum ratings

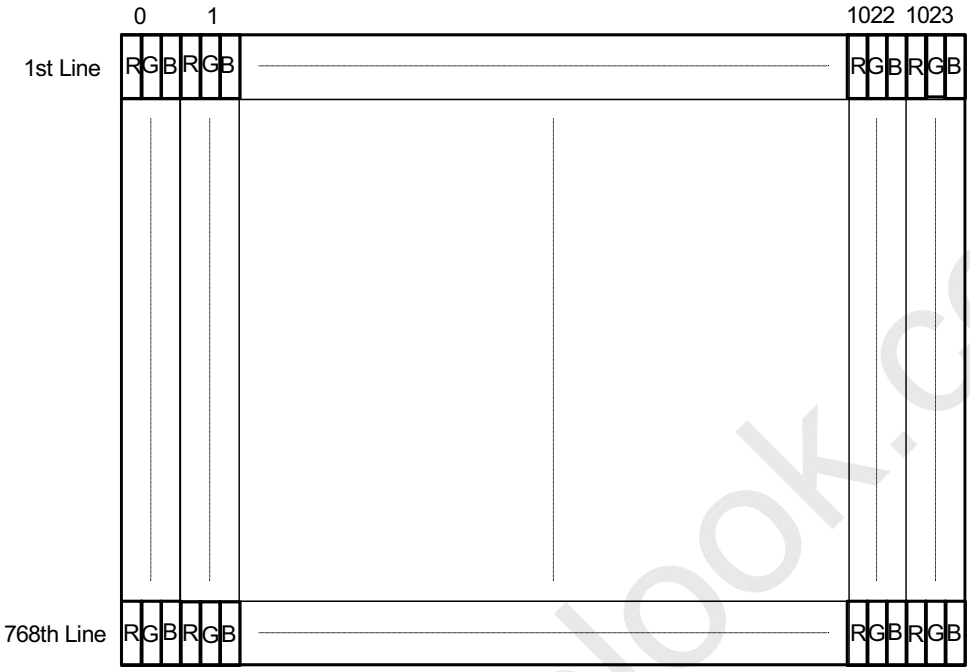
Item	Symbol	Min	Max	Unit	Conditions
Supply Voltage	VDD	-0.3	+4.0	V	
	5VSUS 5VALW	-0.3	+5.5	V	
	PWR_SRC	-0.3	+25	V	
Input Voltage of Signal	Logic input signals(LVDS, EDID, BISTEN)	-0.3	VDD+0.3	V	
	FPVEE	-0.3	5.5	V	
	SMB_CLK SMB_DAT	-1.0	7.0	V	
Operating Temperature	TOP	0	+50	deg. C	(Note)
Operating Humidity	HOP	8	95	%RH	(Note)
Storage Temperature	TST	-20	+60	deg. C	(Note)
Storage Humidity	HST	5	95	%RH	(Note)
Vibration			1.5 10-200	G Hz	
Shock			50 18	G ms	Rectangle Wave

Note: Maximum Wet-Bulb should be 39 degree C and No condensation.

4. Pixel Format Image

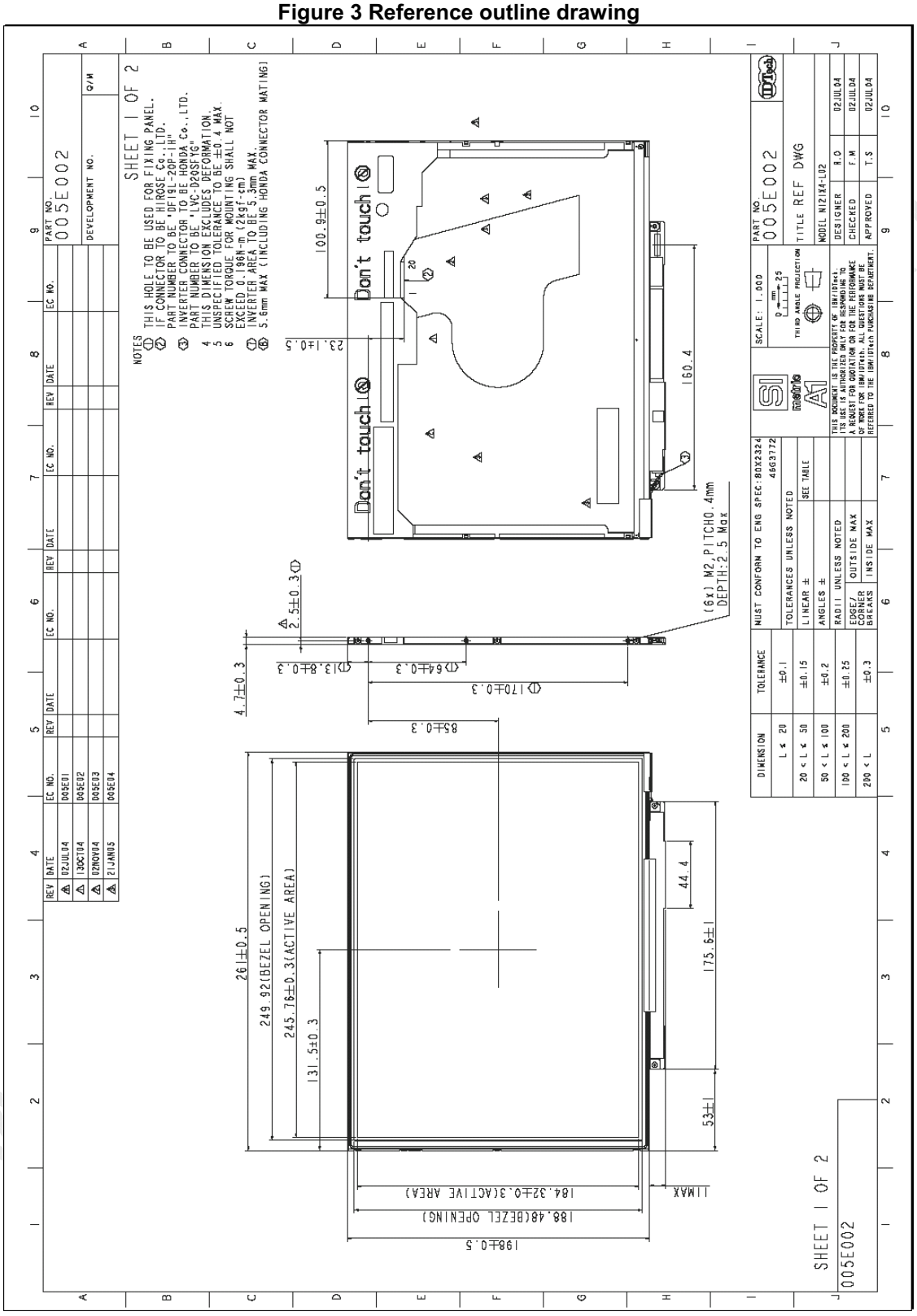
Figure 2 shows the relationship of the input signals and LCD pixel format image.

Figure 2 Pixel Format



5. Mechanical Characteristics

Figure 3 Reference outline drawing



6. Optical Characteristics

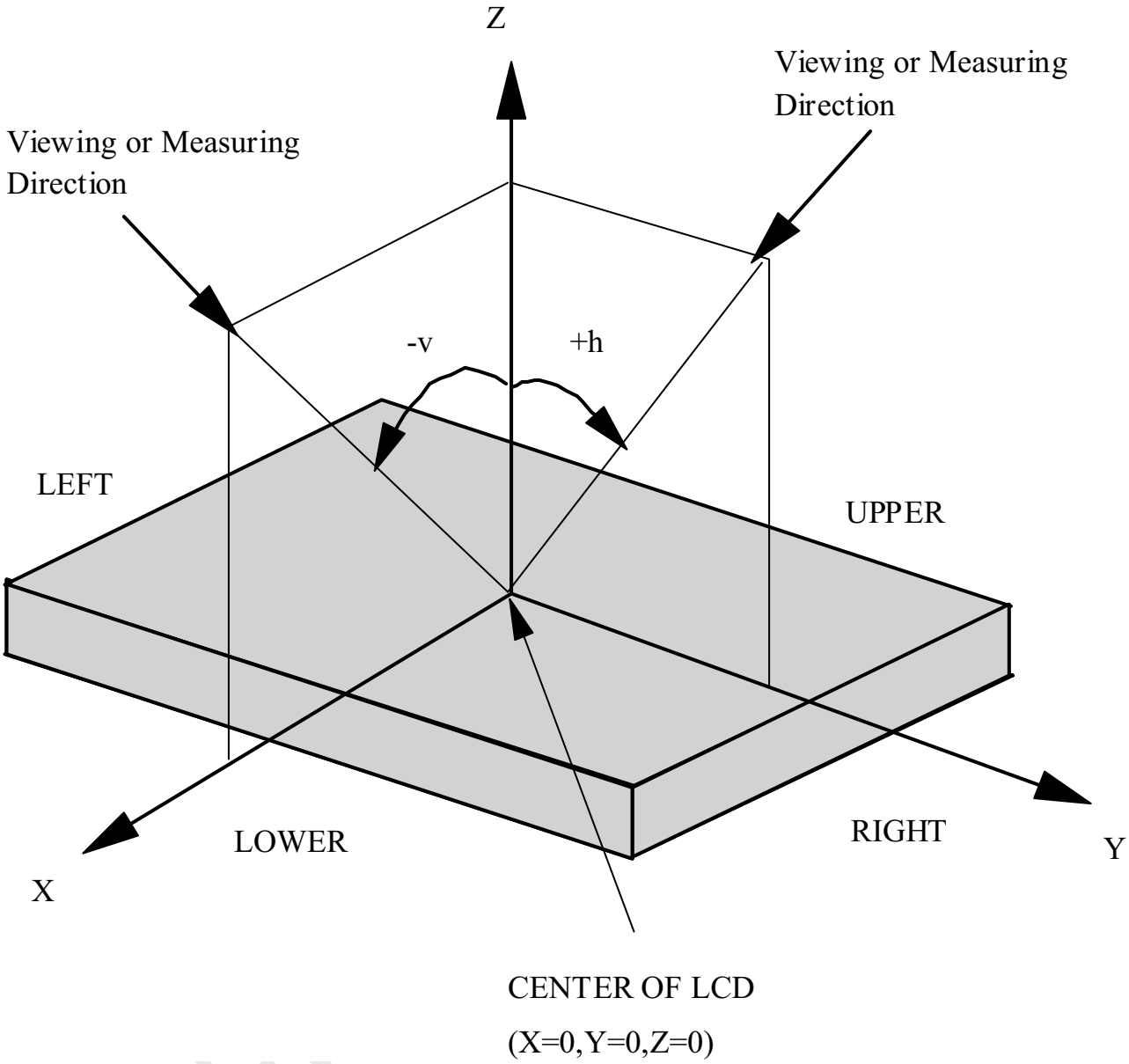
6.1 Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degree C condition:

Table 3 Optical characteristics

Item	Conditions	Specification			
		Min	Typ.	Max	Note
Viewing Angle (Degrees)	Horizontal (Right) K>10(Left)	40 40	- -	- -	
K: Contrast Ratio	Vertical (Upper) K>10 (Lower)	15 30	- -	- -	
Contrast ratio		230	300	-	
Response Time(ms)	Rising + Falling	-	-	50	
Color Chromaticity(CIE)	Red x	0.558	0.584	0.610	+/-0.026
	Red y	0.308	0.336	0.364	+/-0.028
	Green x	0.296	0.322	0.348	+/-0.026
	Green y	0.506	0.534	0.562	+/-0.028
	Blue x	0.125	0.151	0.177	+/-0.026
	Blue y	0.100	0.128	0.156	+/-0.028
	White x	0.287	0.313	0.339	+/-0.026
	White y	0.301	0.329	0.357	+/-0.028
White Luminance(cd/m2)	5 Points average SMData=00H	127	150		

Figure 4 Note for the Optical Characteristics



- Chromaticity and White Balance are defined as the C.I.E. 1931 x,y coordinates at the center of LCD. The Standard Equipments are as shown below table.

Table 4 Standard Equipments

Item	Standard Equipment
Viewing Angle	MCPD-7000 by Ohtsuka Elec.
Contrast	MCPD-7000 by Ohtsuka Elec.
Response Time	BM5A by TOPCON OPTICAL Co.,Ltd.
White Luminance	MCPD-7000 by Ohtsuka Elec.
Luminance Uniformity	MCPD-7000 by Ohtsuka Elec.
Chromaticity	MCPD-7000 by Ohtsuka Elec.
White Balance	MCPD-7000 by Ohtsuka Elec.

The measurement is to be done after 30 minutes of Power-on of Backlight.
Unless otherwise specified, the ambient conditions are as following.

Table 5 Ambient conditions

Ambient Temperature	25 +/-2 (deg C)
Ambient Humidity	25 to 85 (%)
Atmospheric Pressure	86.0 to 104.0 (kPa)

6.2 Luminance Uniformity

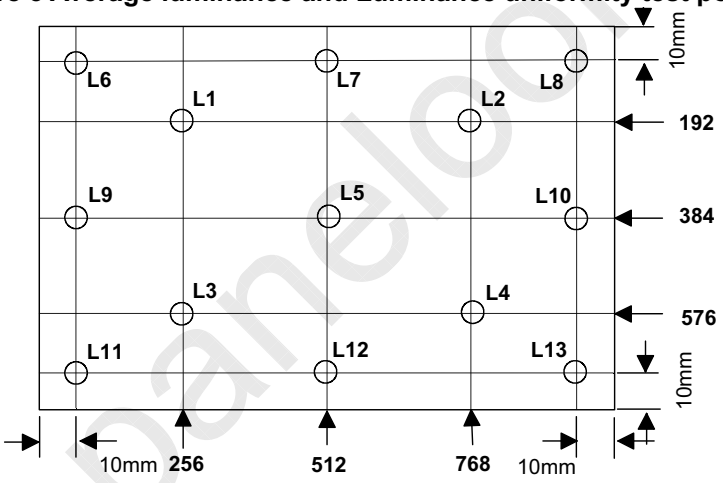
When backlight is on with all pixels in the unselected state(white raster), average luminance and luminance uniformity(variation) is defined as below.

$$\text{Average Luminance} = \frac{L1 + L2 + L3 + L4 + L5}{5}$$

$$\text{UNF(5pts)} = \frac{\max(L1, L2, \cdots L5)}{\min(L1, L2, \cdots L5)} \leq 1.25$$

$$\text{UNF(13pts)} = \frac{\max(L1, L2, \cdots L13)}{\min(L1, L2, \cdots L13)} \leq 1.65$$

Figure 5 Average luminance and Luminance uniformity test points



7. Electrical Characteristics

7.1 Interface Connector

Table 6 Connector Name / Designation

Manufacturer	HIROSE
Type / Part Number	DF19L-20P-1H
Mating Receptacle/Part Number	DF19G-20S-1F (FPC Type) DF19G-20S-1C (Cable Type)

Table 7 Signal pin assignment

Pin #	Signal Name	Description	Remarks
1	GND	Ground	
2	VDD	+3.3V Power Supply	
3	VDD		
4	VEDID	EEDID 3.3V Power Supply	Power source shall be the limited current circuit that has not exceeding 1A. Refer to "Enhanced Display Data Channel (E-DDCTM) Proposed Standard", VESA.
5	BISTEN	BIST(Built-In Self Test) enable	L: Normal operation H: BIST enable See 7.7BIST for detail.
6	ClkEDID	EEDID Clock	CLKEEDID line and DATAEEDID line are pulled up with 10k ohm resistor to VEEDID power source line at LCD panel, respectively.
7	DataEDID (Note 2, 4)	EEDID Data	
8	RxIN0-	LVDS differential data input (Red0-Red5, Green0)	Has 100ohm termination resistor
9	RxIN0+		
10	GND	Ground	
11	RxIN1-	LVDS differential data input (Green1-Green5, Blue0-Blue1)	Has 100ohm termination resistor
12	RxIN1+		
13	GND	Ground	
14	RxIN2-	LVDS differential data input (Blue2-Blue5, HSync, VSync, DSPTMG)	Has 100ohm termination resistor
15	RxIN2+		
16	GND	Ground	
17	RxCLKIN-	LVDS differential clock input	Has 100ohm termination resistor
18	RxCLKIN+		
19	GND	Ground	
20	GND	Ground	

All input signals shall be low or Hi-Z state when VDD is off.

Table 8 Interface Signal Descriptions

SIGNAL NAME	Description	
+RED5	Red Data 5 (MSB)	Red-pixel Data
+RED4	Red Data 4	Each red pixel's brightness data consists of these 6 bits pixel data.
+RED3	Red Data 3	
+RED2	Red Data 2	
+RED1	Red Data 1	
+RED0	Red Data 0 (LSB)	
+GREEN 5	Green Data 5 (MSB)	Green-pixel Data
+GREEN 4	Green Data 4	Each green pixel's brightness data consists of these 6 bits pixel data.
+GREEN 3	Green Data 3	
+GREEN 2	Green Data 2	
+GREEN 1	Green Data 1	
+GREEN 0	Green Data 0 (LSB)	
+BLUE 5	Blue Data 5 (MSB)	Blue-pixel Data
+BLUE 4	Blue Data 4	Each blue pixel's brightness data consists of these 6 bits pixel data.
+BLUE 3	Blue Data 3	
+BLUE 2	Blue Data 2	
+BLUE 1	Blue Data 1	
+BLUE 0	Blue Data 0 (LSB)	
-DTCLK	Data Clock	The typical frequency is 56MHz. The signal is used to strobe the pixel data.
DSPTMG	Display Timing	When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	Vertical Sync	
HSYNC	Horizontal Sync	

7.2 LVDS Receiver

7.2.1. Signal Electrical Characteristics for LVDS Receiver

The built-in LVDS receiver is compatible with ANSI/TIA/TIA-644 standard.

Table 9 LVDS Receiver Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Differential Input High Threshold	Vth			+100	mV	Vcm=+1.2V
Differential Input Low Threshold	Vtl	-100			mV	Vcm=+1.2V
Magnitude Differential Input Voltage	|Vid|	100		600	mV	
Common Mode Voltage	Vcm	1.0	1.2	1.4	V	Vth - Vtl = 200mV
Common Mode Voltage Offset	ΔVcm	-50		+50	mV	Vth - Vtl = 200mV

Note:
- Input signals shall be low or Hi-Z state when VDD is off.
- All electrical characteristics for LVDS signal are defined and shall be measured at the interface connector of LCD.

Parameter	Symbol	min	typ	max	unit
Input low voltage	VIL	0		0.3VDD	V
Input high voltage	VIH	0.7VDD		VDD	V
Input leakage current	IIZ	-10		10	uA

Table 10 Timing Requirements

Parameter	Symbol	Min	Typ	Max	Unit	Conditions	Note
Clock Frequency	fc	50	56	67	MHz		VESA XGA CVT reduced blanking
Cycle Time	tc	14.93	17.86	20.00	ns		
Data Setup Time	Tsu	600			ps	fc = 56MHz	(See Figure 9)
Data Hold Time	Thd	600			ps	tCCJ < 50ps Vth-Vtl = 200m Vcm = 1.2V ΔVcm = 0	(See Figure 9)
Cycle-to-cycle jitter	tCCJ	-150		+150	ps	fc = 56MHz Tsu=Thd=600ps	Jitter is the magnitude of the change in input clock period.
Cycle Modulation Rate	tCJavg			20	ps/clk	fc = 56MHz Tsu=Thd=600ps	tCJavg is maximum average cycle modulation rate in peak-to-peak transition within any 100-clock cycles. Figure 10 Cycle Modulation Rate illustrates a case against this requirement. This specification is applied only if input clock peak jitter within any 100-clock cycles is greater than 300ps.

Note:.All values are at VDD=3.3V, Ta=25 degree C.

Figure 6 Voltage Definitions

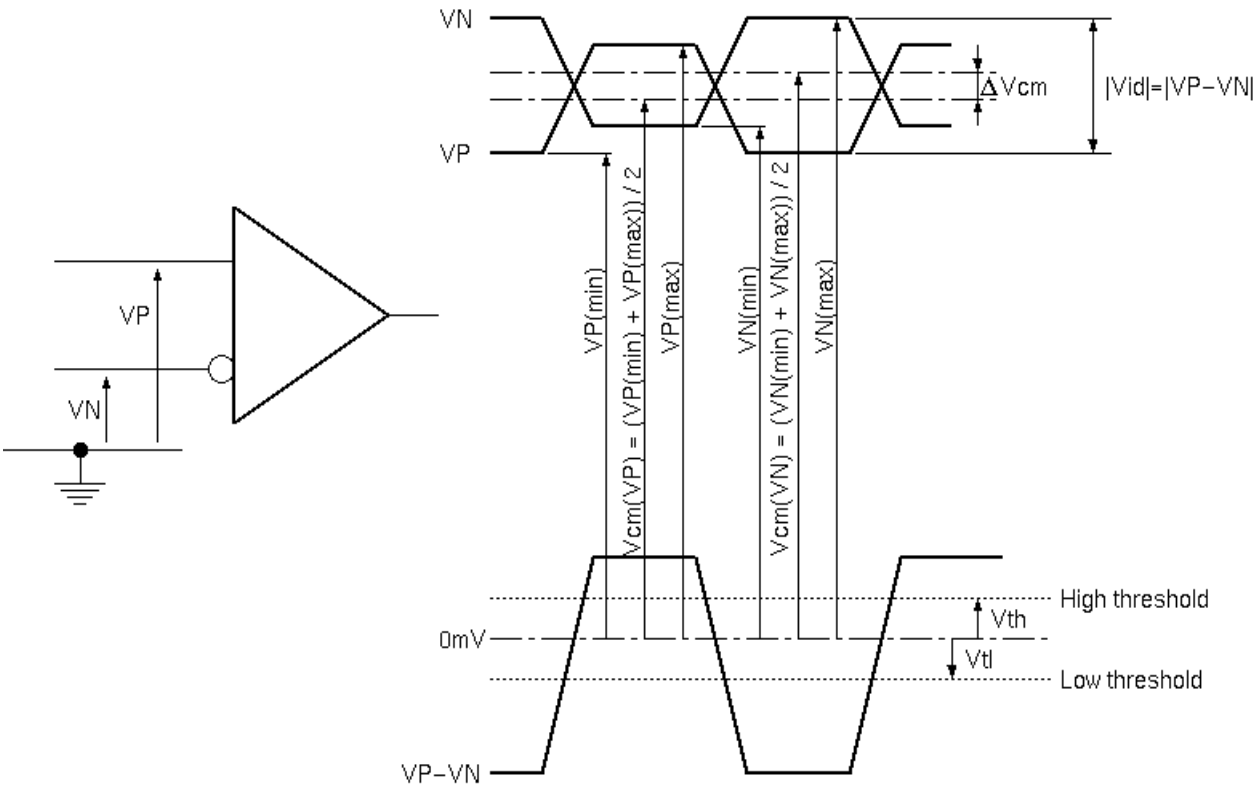


Figure 7 Measurement System

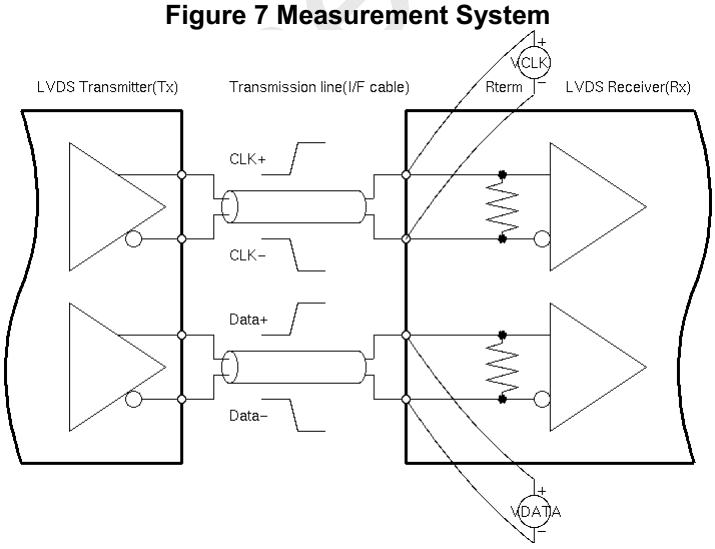


Figure 8 Data mapping

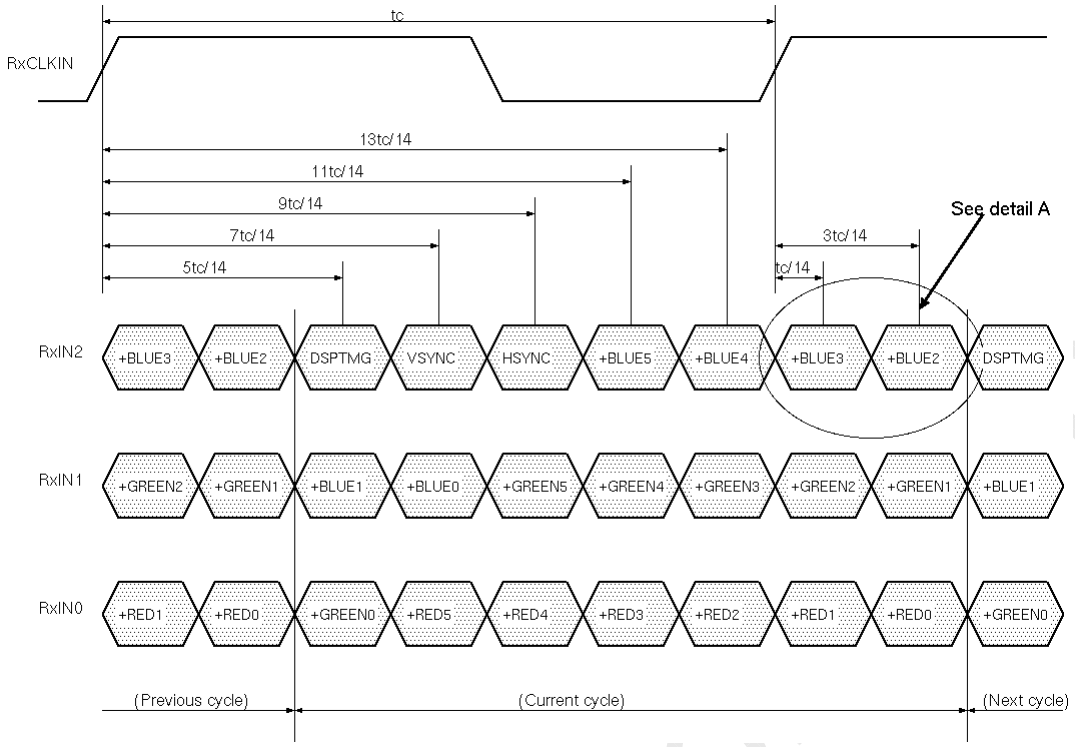
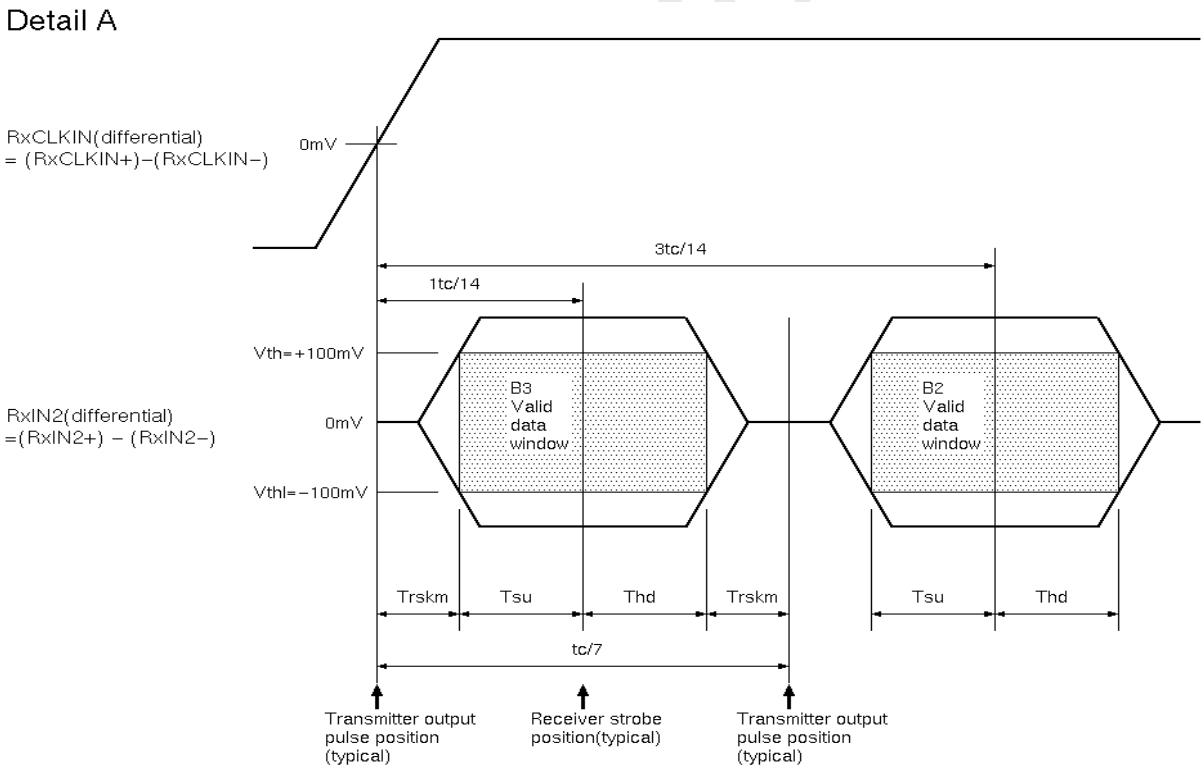
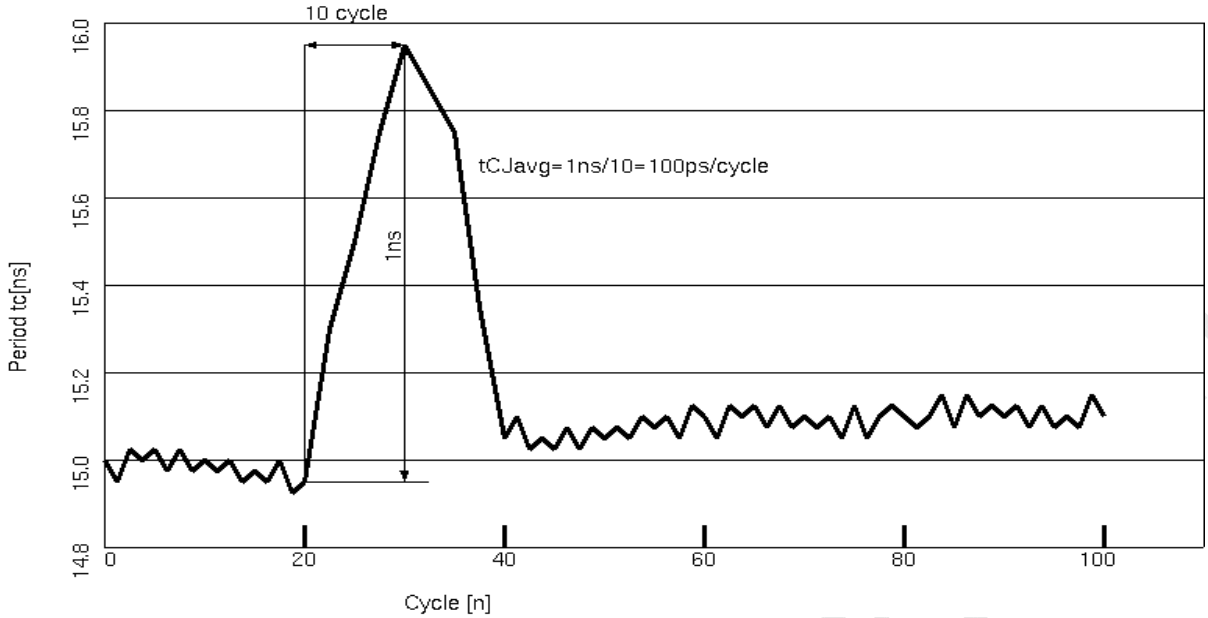


Figure 9 Timing Definition (detail A)



Note: Tsu and Thd are internal data sampling window of receiver. Trskm is the system skew margin; i.e., the sum of cable skew, source clock jitter, and other inter-symbol interference, shall be less than Trskm.

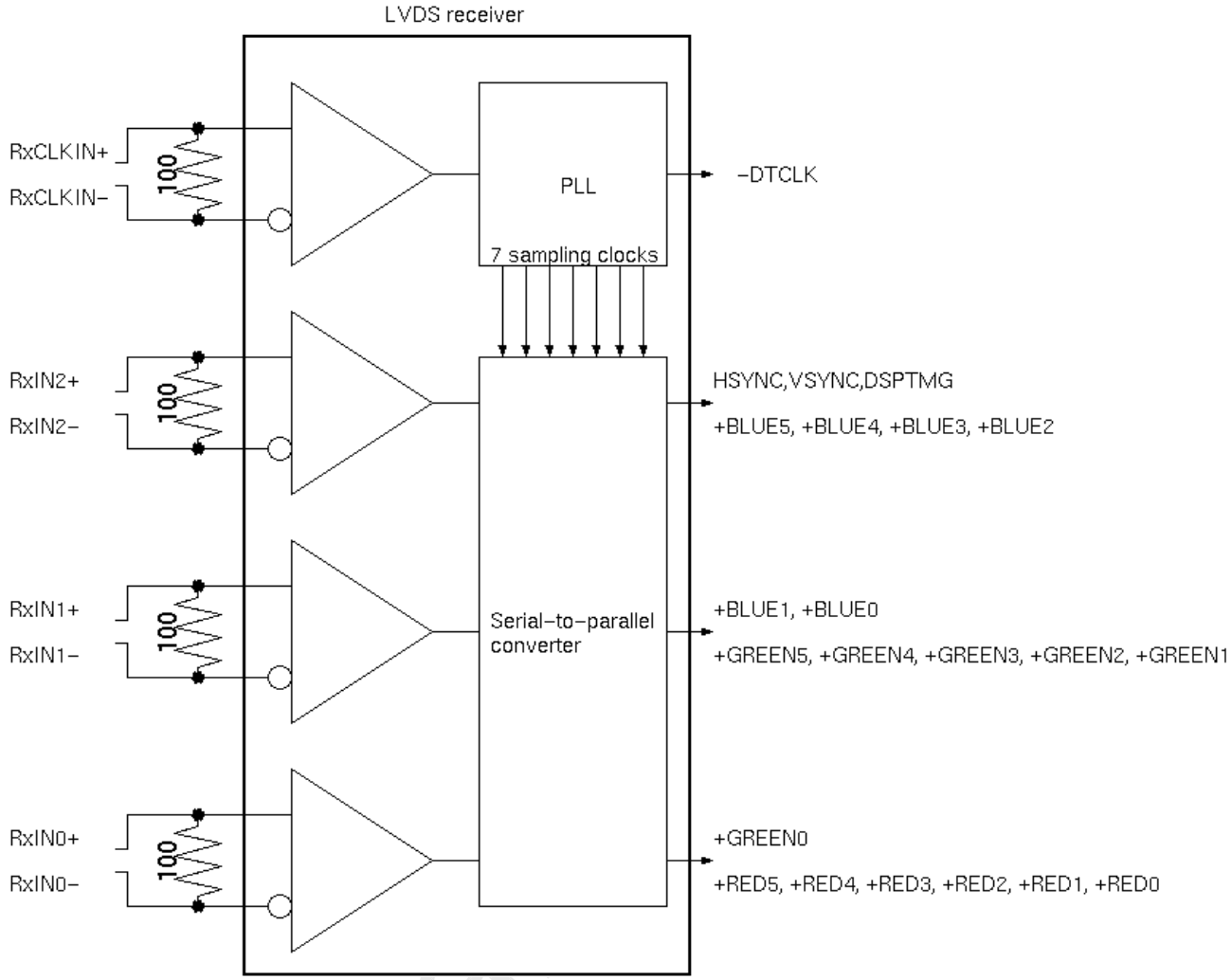
Figure 10 Cycle Modulation Rate



7.2.2. LVDS Receiver Internal Circuit

Figure 11 LVDS Receiver Internal Circuit shows the internal block diagram of the LVDS receiver. This LCD module equips termination resistors for LVDS link.

Figure 11 LVDS Receiver Internal Circuit



7.2.3. Recommended Guidelines for Motherboard PCB Design and Cable Selection

Following the suggestions below will help to achieve optimal results.

- Use controlled impedance media for LADS signals. They should have a matched differential impedance of 100 ohm.
- Match electrical lengths between traces to minimize signal skew.
- Isolate TEL signals from LADS signals.
- For cables, twisted pair, twin, or flex circuit with close coupled differential traces are recommended.

7.3 Interface Timings

VESA CVT reduced blanking timing is supported.
If timing signal is invalid, the LCD enters "self protection mode" and the screen becomes whole black. Once the signal is back, it resumes normal operation.

7.3.1. Timing Characteristics

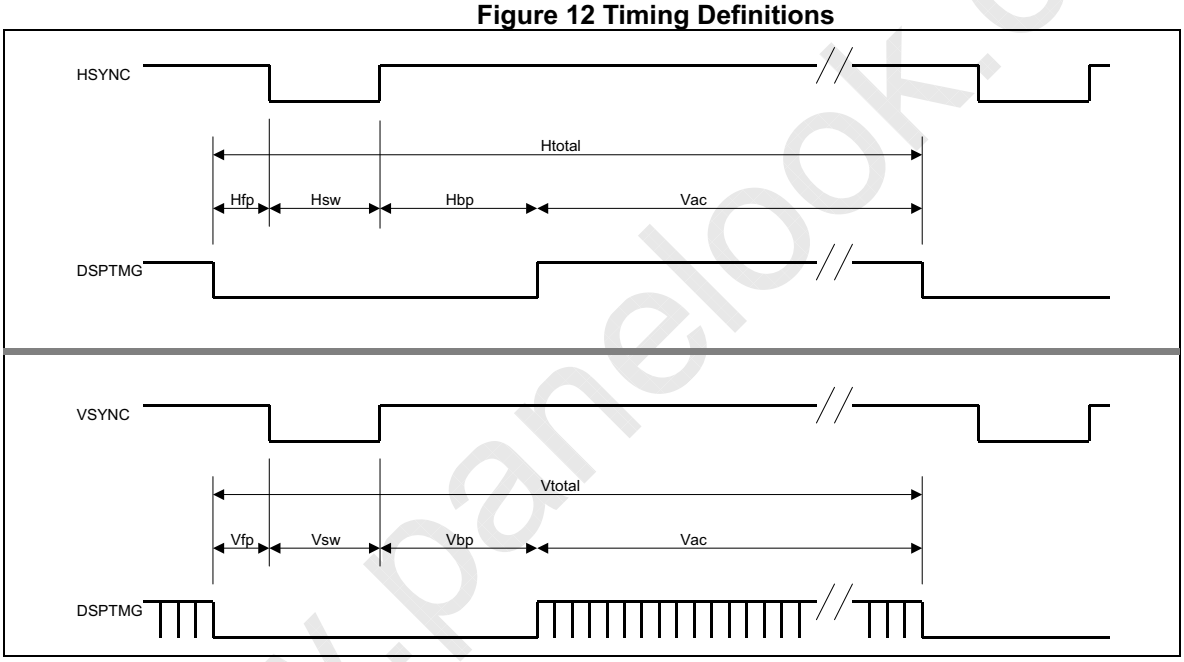
Table 11 Interface timings

Symbol	Parameter	MIN	TYP	MAX	Unit	Note

fdck	DTCLK Frequency		56.00		MHz	See Table 10 Timing Requirements
tck	DTCLK cycle time		17.86		nsec	
Htotal	H total time	1170	1184	2047	tck	
Hac	H active time	1024	1024	1024	tck	
Hsw	H-Sync width	8	32		tck	32 <= Hsw + Hbp < 515 [tck].
Hbp	H back porch	8	80		tck	
Hfp	H front porch	0	48		tck	
Vtotal	V total time	780	790	1023	tx	
Vac	V active time	768	768	768	tx	
Vsync	Frame rate	55	60	61	Hz	
Vsw	V-sync Width	1	4		tx	
Vfp	V-sync front porch	1	3		tx	
Vbp	V-sync back porch	11	15	63	tx	Vbp should be static.

7.3.2. Timing Definition

Figure 12 Timing Definitions



7.4 EEDID

Table 12 EEDID

Supported Standards	VESA ENHANCED EXTENDED DISPLAY IDENTIFICATION DATA STANDARD Release A, Revision 1" and supports "EEDID version 1.3
EEPROM IC	BR24L02F(ROHM) or equivalent
I2C Device Address	A0/A1

Table 13 Data table

Address	Category	Description	Data	Remark
00h	Header	Header	00h	Header, Fixed

01h	Header	Header	FFh	Header, Fixed
02h	Header	Header	FFh	Header, Fixed
03h	Header	Header	FFh	Header, Fixed
04h	Header	Header	FFh	Header, Fixed
05h	Header	Header	FFh	Header, Fixed
06h	Header	Header	FFh	Header, Fixed
07h	Header	Header	00h	Header, Fixed
08h	Vendor/Product Identification	ID Manufacturer Name	0Dh	EISA Manuf. Code LSB 3 character in compressed ASCII: "CMO -> 0D AF
09h	Vendor/Product Identification	ID Manufacturer Name	AFh	EISA Manuf. Code LSB 3 character in compressed ASCII: "CMO -> 0D AF
0Ah	Vendor/Product Identification	ID Product Code	02h	Panel Supplier Reserved - Product code 12 02
0Bh	Vendor/Product Identification	ID Product Code	12h	Panel Supplier Reserved - Product code 12 02
0Ch	Vendor/Product Identification	ID Serial Number	00h	Optional 32-bit serial no. Unused(00h)
0Dh	Vendor/Product Identification	ID Serial Number	00h	Optional 32-bit serial no. Unused(00h)
0Eh	Vendor/Product Identification	ID Serial Number	00h	Optional 32-bit serial no. Unused(00h)
0Fh	Vendor/Product Identification	ID Serial Number	00h	Optional 32-bit serial no. Unused(00h)
10h	Vendor/Product Identification	Week of Manufacture	00h	Week of manufacture 1 - 53 (unused: 00h)
11h	Vendor/Product Identification	Year of Manufacture	00h	Year of manufacture year - 1990(unsed:00h)
12h	EDID Structure Version/Revision	Version #	01h	Version=1
13h	EDID Structure Version/Revision	Revision #	03h	Revision=3
14h	Basic Display Parameters/Features	Video Input Definition	80h	Signal Level: Digital DFP 1.x: no
15h	Basic Display Parameters/Features	Max. Horitonal Image Size	19h	Horizontal active area, rounded to nearest centimeter. 24.576cm -> 19h
16h	Basic Display Parameters/Features	Max. Vertical Image Size	12h	Vertical active area, rounded to nearest centimeter. 18.432cm -> 12h
17h	Basic Display Parameters/Features	Display Transfer Characteristics(Gamma)	78h	gamma=2.2 (gamma * 100-100 = 2.2*100-100 = 120 = 78h)
18h	Basic Display Parameters/Features	Feature Support	0Ah	DPMS:no Active off:no Type:RGB-color sRGB:no Preferred Timing Mode:yes GTF:no
19h	Color Characteristics	Red/Green(D1-D0	E7h	Rx1 Rx0 Ry1 Ry0 Gx1 Gx0 Gy1 Gy0
1Ah	Color Characteristics	Blue/White(D1-D0)	B5h	Bx1 Bx0 By1 By0 Wx1 Wx0 Wy1 Wy0
1Bh	Color Characteristics	Red-x(D9-D2)	93h	Rx=0.577
1Ch	Color Characteristics	Red-y(D9-D2)	56h	Ry=0.338
1Dh	Color Characteristics	Green-x(D9-D2)	4Fh	Gx=0.310
1Eh	Color Characteristics	Green-y(D9-D2)	8Dh	Gy=0.554
1Fh	Color Characteristics	Blue-x(D9-D2)	28h	Bx=0.158

20h	Color Characteristics	Blue-y(D9-D2)	1Fh	By=0.124
21h	Color Characteristics	White-x(D9-D2)	50h	Wx=0.313
22h	Color Characteristics	White-y(D9-D2)	54h	Wy=0.329
23h	Established Timings	Established Timings 1	00h	Not supported
24h	Established Timings	Established Timings 2	00h	Not supported
25h	Established Timings	Manufacturer's Reserved Timings	00h	No manufacturer's specific timing
26h	Standard Timing Identification	Standard Timing Identification #1	01h	(Established timing: Hactive / 8 - 31 = 1024/8-31)
27h	Standard Timing Identification	Standard Timing Identification #1	01h	(Established timing: Image aspect ratio=4:3 Refresh rate=60Hz)
28h	Standard Timing Identification	Standard Timing Identification #2	01h	01h: Blank
29h	Standard Timing Identification	Standard Timing Identification #2	01h	01h: Blank
2Ah	Standard Timing Identification	Standard Timing Identification #3	01h	01h: Blank
2Bh	Standard Timing Identification	Standard Timing Identification #3	01h	01h: Blank
2Ch	Standard Timing Identification	Standard Timing Identification #4	01h	01h: Blank
2Dh	Standard Timing Identification	Standard Timing Identification #4	01h	01h: Blank
2Eh	Standard Timing Identification	Standard Timing Identification #5	01h	01h: Blank
2Fh	Standard Timing Identification	Standard Timing Identification #5	01h	01h: Blank
30h	Standard Timing Identification	Standard Timing Identification #6	01h	01h: Blank
31h	Standard Timing Identification	Standard Timing Identification #6	01h	01h: Blank
32h	Standard Timing Identification	Standard Timing Identification #7	01h	01h: Blank
33h	Standard Timing Identification	Standard Timing Identification #7	01h	01h: Blank
34h	Standard Timing Identification	Standard Timing Identification #8	01h	01h: Blank
35h	Standard Timing Identification	Standard Timing Identification #8	01h	01h: Blank
36h	Detailed Timing Descriptions	Detailed Timing Description #1	E0h	Pixel clock/10000(D7-D0) 56MHz/10000 = 5600 = 15E0h
37h	Detailed Timing Descriptions	Detailed Timing Description #1	15h	Pixel clock/10000(D15-D8) 56MHz/10000 = 5600 = 15E0h
38h	Detailed Timing Descriptions	Detailed Timing Description #1	00h	HActive(D7-D0) = 1024 mod 256 = 00h
39h	Detailed Timing Descriptions	Detailed Timing Description #1	A0h	HBlank(D7-D0) = 160 mod 256 = A0h
3Ah	Detailed Timing Descriptions	Detailed Timing Description #1	40h	HActive(D11-D8) : HBlank(D11-D8) = 1024/256 : 160/256 = 40h
3Bh	Detailed Timing Descriptions	Detailed Timing Description #1	00h	VActive(D7-D0) = 768 mod 256
3Ch	Detailed Timing Descriptions	Detailed Timing Description #1	16h	VBlank(D7-D0) = 22 mod 256 = 16h
3Dh	Detailed Timing Descriptions	Detailed Timing Description #1	30h	VActive(D11-D8) : VBlank(D11-D8) = 768/256 : 22 / 256 = 30h
3Eh	Detailed Timing Descriptions	Detailed Timing Description #1	30h	HSyncOffset(D7-D0) = HBorder+HFrontPorch = 48 = 30h
3Fh	Detailed Timing Descriptions	Detailed Timing Description #1	20h	HSyncWidth(D7-D0) = 32 = 20h

40h	Detailed Timing Descriptions	Detailed Timing Description #1	34h	VSyncOffset(D3-D0) : VSyncWidth(D3-D0) = 3:4 = 34h
41h	Detailed Timing Descriptions	Detailed Timing Description #1	00h	HSyncOffset(D9-D8) : HSyncWidth(D9-D8) : VSyncOffset(D5-D4) : VSyncWidth(D5-D4) = 0:0:0:0 = 00h
42h	Detailed Timing Descriptions	Detailed Timing Description #1	F6h	HImageSize(mm, D7-D0) = 245.76mm = F6h
43h	Detailed Timing Descriptions	Detailed Timing Description #1	B8h	VImageSize(mm, D7-D0) = 184.32mm = B8h
44h	Detailed Timing Descriptions	Detailed Timing Description #1	00h	HImageSize(D11-D8) : VImageSize(D11-D8)
45h	Detailed Timing Descriptions	Detailed Timing Description #1	00h	HBorder=0(Zero for notebook LCD)
46h	Detailed Timing Descriptions	Detailed Timing Description #1	00h	VBorder=0(Zero for notebook LCD)
47h	Detailed Timing Descriptions	Detailed Timing Description #1	18h	Non-interlaced, Normal Display, Digital separate, Negative V/H sync porality, no DE-only mode support
48h	Detailed Timing Descriptions	Detailed Timing Description #2	00h	Timimg Descriptor #2 Alternate Panel Timing -- not used
49h	Detailed Timing Descriptions	Detailed Timing Description #2	00h	
4Ah	Detailed Timing Descriptions	Detailed Timing Description #2	00h	
4Bh	Detailed Timing Descriptions	Detailed Timing Description #2	00h	
4Ch	Detailed Timing Descriptions	Detailed Timing Description #2	00h	
4Dh	Detailed Timing Descriptions	Detailed Timing Description #2	00h	
4Eh	Detailed Timing Descriptions	Detailed Timing Description #2	00h	
4Fh	Detailed Timing Descriptions	Detailed Timing Description #2	00h	
50h	Detailed Timing Descriptions	Detailed Timing Description #2	00h	
51h	Detailed Timing Descriptions	Detailed Timing Description #2	00h	
52h	Detailed Timing Descriptions	Detailed Timing Description #2	00h	
53h	Detailed Timing Descriptions	Detailed Timing Description #2	00h	
54h	Detailed Timing Descriptions	Detailed Timing Description #2	00h	
55h	Detailed Timing Descriptions	Detailed Timing Description #2	00h	
56h	Detailed Timing Descriptions	Detailed Timing Description #2	00h	
57h	Detailed Timing Descriptions	Detailed Timing Description #2	00h	
58h	Detailed Timing Descriptions	Detailed Timing Description #2	00h	
59h	Detailed Timing Descriptions	Detailed Timing Description #2	00h	
5Ah	Detailed Timing Descriptions	Detailed Timing Description #3	00h	Header flag 00h
5Bh	Detailed Timing Descriptions	Detailed Timing Description #3	00h	Header flag 00h
5Ch	Detailed Timing Descriptions	Detailed Timing Description #3	00h	Header flag 00h
5Dh	Detailed Timing Descriptions	Detailed Timing Description #3	FEh	Header Data type tag(Monitor) ASCII String FEh
5Eh	Detailed Timing Descriptions	Detailed Timing Description #3	00h	Header flag 00h
5Fh	Detailed Timing Descriptions	Detailed Timing Description #3	55h	Dell P/N 1st Character - "U"
60h	Detailed Timing Descriptions	Detailed Timing Description #3	35h	Dell P/N 1st Character - "5"
61h	Detailed Timing Descriptions	Detailed Timing Description #3	31h	Dell P/N 1st Character - "1"

62h	Detailed Timing Descriptions	Detailed Timing Description #3	32h	Dell P/N 1st Character - "2"
63h	Detailed Timing Descriptions	Detailed Timing Description #3	32h	Dell P/N 1st Character - "2"
64h	Detailed Timing Descriptions	Detailed Timing Description #3	03h	LCD Supplier EEDID Revision #: X02 -> 03h
65h	Detailed Timing Descriptions	Detailed Timing Description #3	4Eh	Manufacturer model name "N121X4" - "N"
66h	Detailed Timing Descriptions	Detailed Timing Description #3	31h	Manufacturer model name "N121X4" - "1"
67h	Detailed Timing Descriptions	Detailed Timing Description #3	32h	Manufacturer model name "N121X4" - "2"
68h	Detailed Timing Descriptions	Detailed Timing Description #3	31h	Manufacturer model name "N121X4" - "1"
69h	Detailed Timing Descriptions	Detailed Timing Description #3	58h	Manufacturer model name "N121X4" - "X"
6Ah	Detailed Timing Descriptions	Detailed Timing Description #3	34h	Manufacturer model name "N121X4" - "4"
6Bh	Detailed Timing Descriptions	Detailed Timing Description #3	0Ah	Empty: 20h(if <13 char, terminate with 0Ah, remaining char =20h)
6Ch	Detailed Timing Descriptions	Detailed Timing Description #4	00h	Flag: 00h when block used as monitor descriptor
6Dh	Detailed Timing Descriptions	Detailed Timing Description #4	00h	Flag: 00h when block used as monitor descriptor
6Eh	Detailed Timing Descriptions	Detailed Timing Description #4	00h	Reserved: 00h when block used as monitor descriptor
6Fh	Detailed Timing Descriptions	Detailed Timing Description #4	FEh	Data tag: FEh(ASCII string)
70h	Detailed Timing Descriptions	Detailed Timing Description #4	00h	Flag: 00h when block used as descriptor
71h	Detailed Timing Descriptions	Detailed Timing Description #4	E5h	SMBUS value @10[cd/m2] = E5h
72h	Detailed Timing Descriptions	Detailed Timing Description #4	D1h	SMBUS value @17[cd/m2] = D1h
73h	Detailed Timing Descriptions	Detailed Timing Description #4	C3h	SMBUS value @24[cd/m2] = C3h
74h	Detailed Timing Descriptions	Detailed Timing Description #4	BAh	SMBUS value @30[cd/m2] = BAh
75h	Detailed Timing Descriptions	Detailed Timing Description #4	91h	SMBUS value @60[cd/m2] = 91h
76h	Detailed Timing Descriptions	Detailed Timing Description #4	6Ch	SMBUS value @90[cd/m2] = 6Ch
77h	Detailed Timing Descriptions	Detailed Timing Description #4	44h	SMBUS value @120[cd/m2] = 44h
78h	Detailed Timing Descriptions	Detailed Timing Description #4	00h	SMBUS value @150[cd/m2] = 00h
79h	Detailed Timing Descriptions	Detailed Timing Description #4	01h	Number of LVDS receiver chip = 1
7Ah	Detailed Timing Descriptions	Detailed Timing Description #4	01	BIST Enable: Yes=01h
7Bh	Detailed Timing Descriptions	Detailed Timing Description #4	0Ah	Terminator 0Ah
7Ch	Detailed Timing Descriptions	Detailed Timing Description #4	20h	Empty: 20h
7Dh	Detailed Timing Descriptions	Detailed Timing Description #4	20h	Empty: 20h
7Eh	Extension Flag	Extension Flag	00h	No extension
7Fh	Checksum	Checksum	EEh	One-byte checksum of entire 128 bytes EDED equals 00h.

7.5 Power Consumption

Table 14 shows input power specifications.

Table 14 Power consumption

SYMBOL	PARAMETER	Min	Typ	Max	UNITS	CONDITION
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[V]	Load Capacitance 20[uF]
PDD	VDD Power			1.2	[W]	Max pattern VDD=3.6[V]
PDD	VDD Power		0.9		[W]	All Black Pattern VDD=3.3[V]
IDD	VDD Current			340	[mA]	Max Pattern VDD=3.6[V]
IDD	VDD Current		250		[mA]	All Black Pattern VDD=3.3[V]
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mVp-p]	

7.6 Power ON/OFF Sequence

Figure 13 and Table 15 show VDD power and lamp on/off sequence requirements.
Signals from any system shall be Hi-Z state or low level when VDD is off.

Figure 13 Power sequence

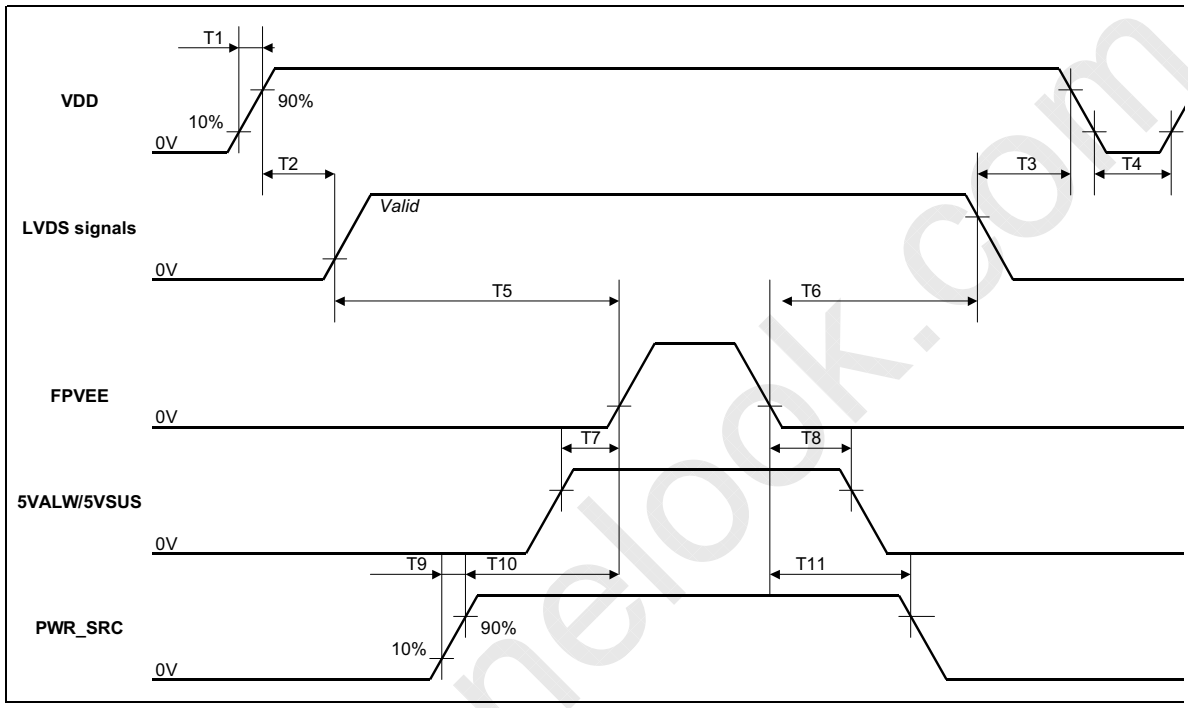


Table 15 Power Sequencing Requirements

Parameter	Symbol	Unit	min	typ	max
VDD rise time	T1	ms	0.5	-	10
VDD on => signal on	T2	ms	0	-	50
Signal off => VDD off	T3	ms	0	-	50
VDD off	T4	ms	500	-	-
Signal on => B/L on	T5	ms	200	-	-
B/L off => signal off	T6	ms	200	-	-
5VALW/5VSUS on => FPVEE on	T7	ms	0	-	-
FPVEE off => 5VALW/5VSUS off	T8	ms	0	-	-
PWR_SRC rise time	T9	ms	1	-	30
PWR_SRC on => FPVEE on	T10	ms	10	-	-
FPVEE off => PWR_SRC off	T11	ms	0	-	-

7.7 BIST

This LCD has BIST(Built-In Self Test) function.
When in BIST mode, LCD display 5 rotating patterns automatically every two seconds, as shown in “Figure 14 BIST display data patterns”.
To enter BIST mode, BISTEN pin must be set to H and LVDS clock must be suspended. Note that logic level of differential inputs must be stable; i.e., RxCLK+ = L and RxCLK- = H, or vice versa. See “Table 16 Operation mode” and “Figure 15 Entering/leaving BIST mode”.
In any circumstances, do not drive BISTEN to H while VDD is off. Such reverse voltage bias may damage the timing controller LSI.
.

Table 16 Operation mode

	LVDS clock is active	LVDS clock is suspended
BISTEN=L	Normal operation: displays the image from host graphics system.	Self-protection mode: displays whole black screen.
BISTEN=H	If previous state is “normal operation”(BIST=H and LVDS clock is active), continues normal operation. Otherwise, displays all black for five seconds, then enters LCD manufacturer’s test mode. This state is considered “transitional” and should not continue more than 100ms.	BIST mode: displays 5 self-rotating patterns every 2 seconds.

Figure 14 BIST display data patterns

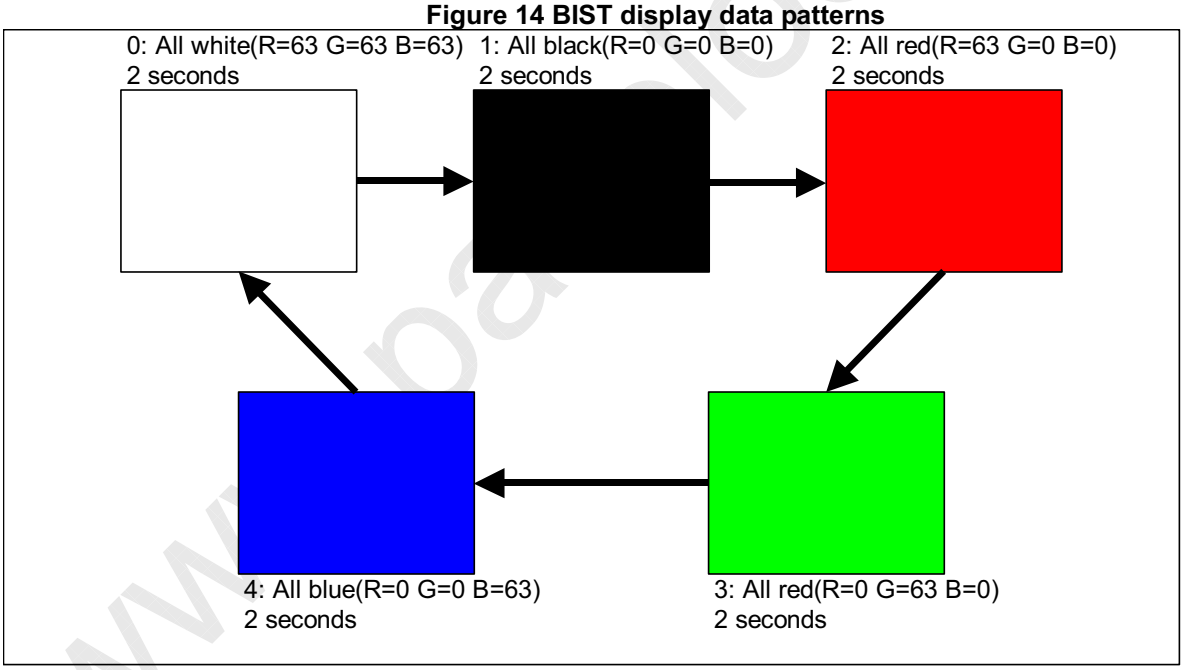
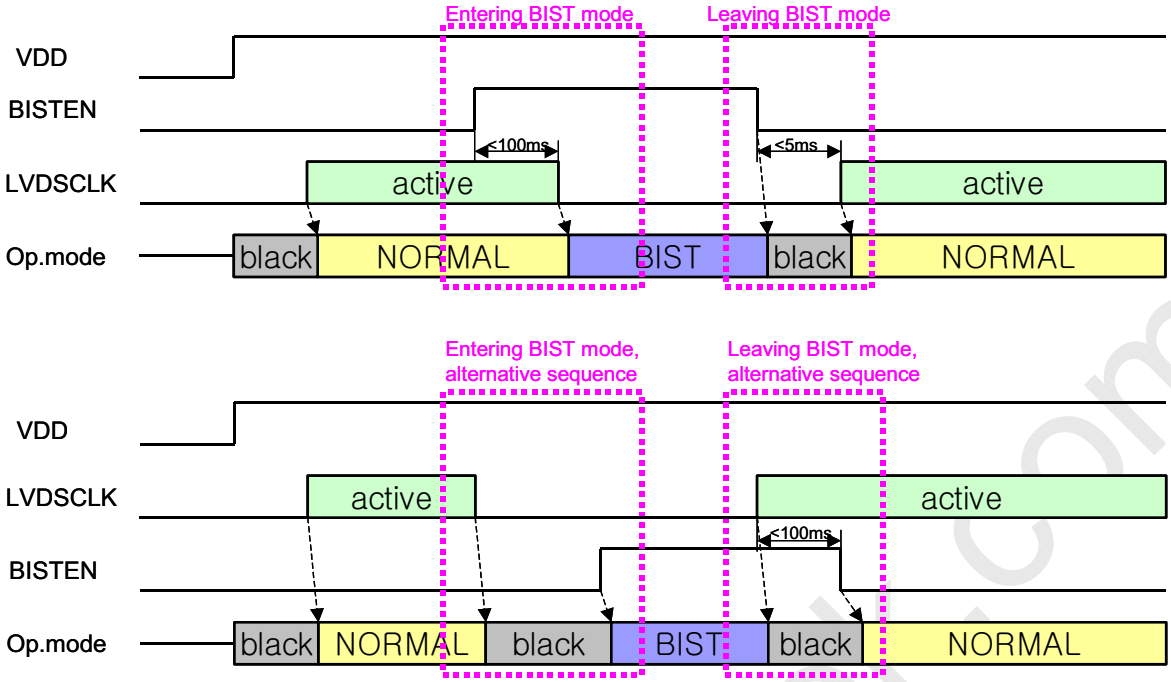


Figure 15 Entering/leaving BIST mode



8. Inverter

8.1 Interface Connector

Table 17 Connector Name / Designation

Manufacturer	HONDA
Type / Part Number	HONDA LVC-D20SFYG3
Mating Type / Part Number	HONDA LVC-C20LPMSG or LVC-D20LPMSG

Table 18 Signal pin assignment

Pin#	Signal Name	Description
1	PWR_SRC	Power rail to drive the backlight inverter
2	PWR_SRC	
3	PWR_SRC	
4	NC	No connection
5	GND	Ground
6	5VSUS	Power source for the control circuit on the inverter.
7	5VALW	Power source for storing the brightness value and for the interfacing with SMB-CLK & SMB-DAT
8	GND	Ground
9	SMB-DAT	SMBus interface for sending brightness information to the inverter
10	SMB-CLK	
11	GND	
12	FPVEE	Control signal input into the inverter to turn the backlight ON/OFF
13	GND	Ground
14	LAMP_STAT	Status output L: Failure H: Good Note: LAMP_STAT is open drain node pulled up with 200Kohms resistor to 5VALW line. DC characteristics of logic low output is: VOL=0.4V max @ IOL=1mA
15	NC	No connection
16	NC	No connection
17	NC	No connection
18	NC	No connection
19	NC	No connection
20	NC	No connection

Note: Output signals from any system shall be low or hi-fi state when VDD is off.

8.2 Electrical Characteristics

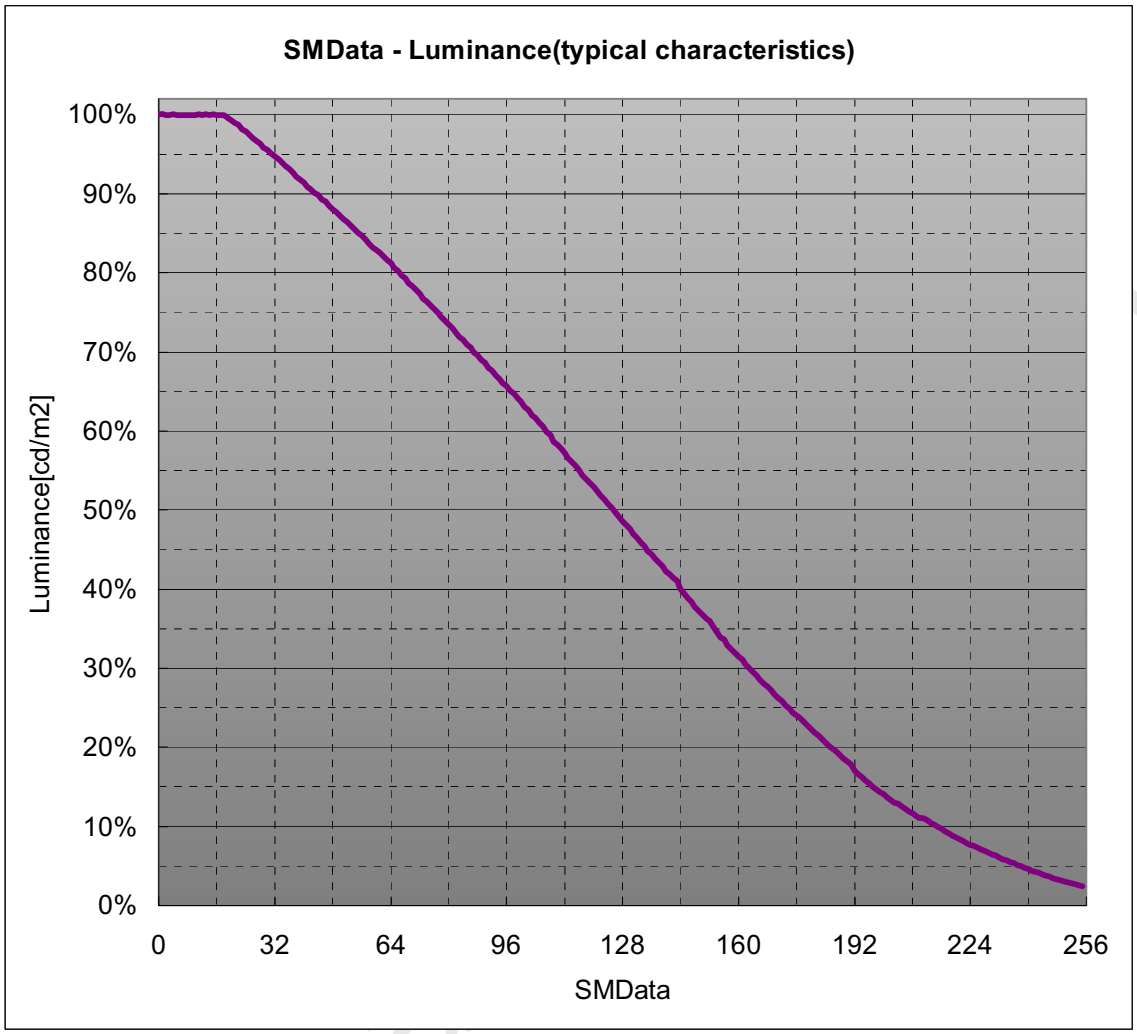
Table 19 Electrical Specifications

Item	Symbol	Min.	Typ.	Max.	UNITS	CONDITION
Input Voltage	PWR_SRC	7.5	14.4	21	[V]	(Ta=25degree C)
	5VSUS, 5VALW	4.85	5.0	5.2	[V]	
Input Power	P(PWR_SRC)		3.9	4.4	[W]	SMData=00H
	PWR_SRC=14.4[V]		0.4	0.6	[W]	SMData=FFH
	P (5VSUS)		50	70	[mW]	
	P (5VALW)		-	10	[mW]	
ON/OFF	FPVEE	2.0			[V]	ON
	FPVEE			0.8	[V]	OFF
Lamp Frequency	F	52	58	66	[KHz]	
Burst Frequency	FB	180	210	240	[Hz]	

Table 20 SMBUS Data

SMBUS	Device Identifier	Device Address
	0101	100

Figure 16 SMData – Luminance



9. Qualifications and CFL Life

This Quality Specification is supplied from CHI MEI Optoelectronics to the customer.

Please pay attention the following items, when this LCD Module is checked in your inspection.

- You should consider the LCD Module to mount that uneven force is not applied to this LCD Module.
- Do not push and put a label on the rear side that is located backlight.
- Do not joggle the LCD Module, there will be some ripple on the screen.
- Display qualifications depend on the power on time. The visual screen quality is applied the state since 30 seconds after power on.

9.1 Visual Screen Quality

Table 21 shows the visual screen quality of the general TFT-LCD module at power-off.

Table 21 Visual screen quality

Polarizer Scratch/Bubble	Size (mm)	Allowable maximum counts
Elliptical defects	d < 0.2	Disregarded
	0.2 ≦ d < 0.4	5
	0.4 ≦ d	0
Linear defects	w < 0.07	Disregarded
	0.07 ≦ w < 0.1 and l < 3.0	5
	0.1 ≦ w or 3.0 ≦ l	0

- d : diameter, d= (longaxis + shortaxis) / 2
- w : line width
- l : line length

9.2 Line Defect

- No visible line defect is allowed in entire screen.
- A Line Defect is defined as a horizontal and vertical apparent line, visible through 5% ND-filter, that differs from adjacent lines at any gray raster pattern.

9.3 Bright and Black Dots

The following Table describes the specification of bright and black dots in the visual screen quality of the TFT-LCD module at power-ON.

Table 22 Pixel defects

Items	Specification
Any Bright Dots	0
Any Black Dots	8 Max
Bright and Black Dots(total)	8 Max
Two Joined Bright Dots	0
Two Joined Black Dots	3 Pair Max
Three Joined Black Dots	1 Max
Bright/Black Dots Distance (Any Combination)	5 mm Min

Definitions:
1. A Bright Dot is any one of a stuck Red, Green or Blue pixel visible through 5% ND-filter under all black background.
2. A Black Dot is an unlit pixel under any of White, Red, Green or Blue bright raster.
Note : A lit is agreed separately by demonstrated module.
Basic Conditions:

Viewing Distance	350 to 500 mm
Ambient Illumination	300 to 700 lux
Ambient Temperature	20 to 25 degreeC

9.4 CFL Life

Table 23 CFL life

CFL Life Time	10,000 Hours	condition 25 deg.C and 4.5mArms

The assumed CFL Life will be until the luminance becomes 50% of its initial value.

10. Packaging Specifications

- 20 LCD modules / 1 Box
- Box dimensions: 383(L) x 323(W) x 341(H)
- Meets 90 cm drop test

Figure 17 Packaging(type-A)

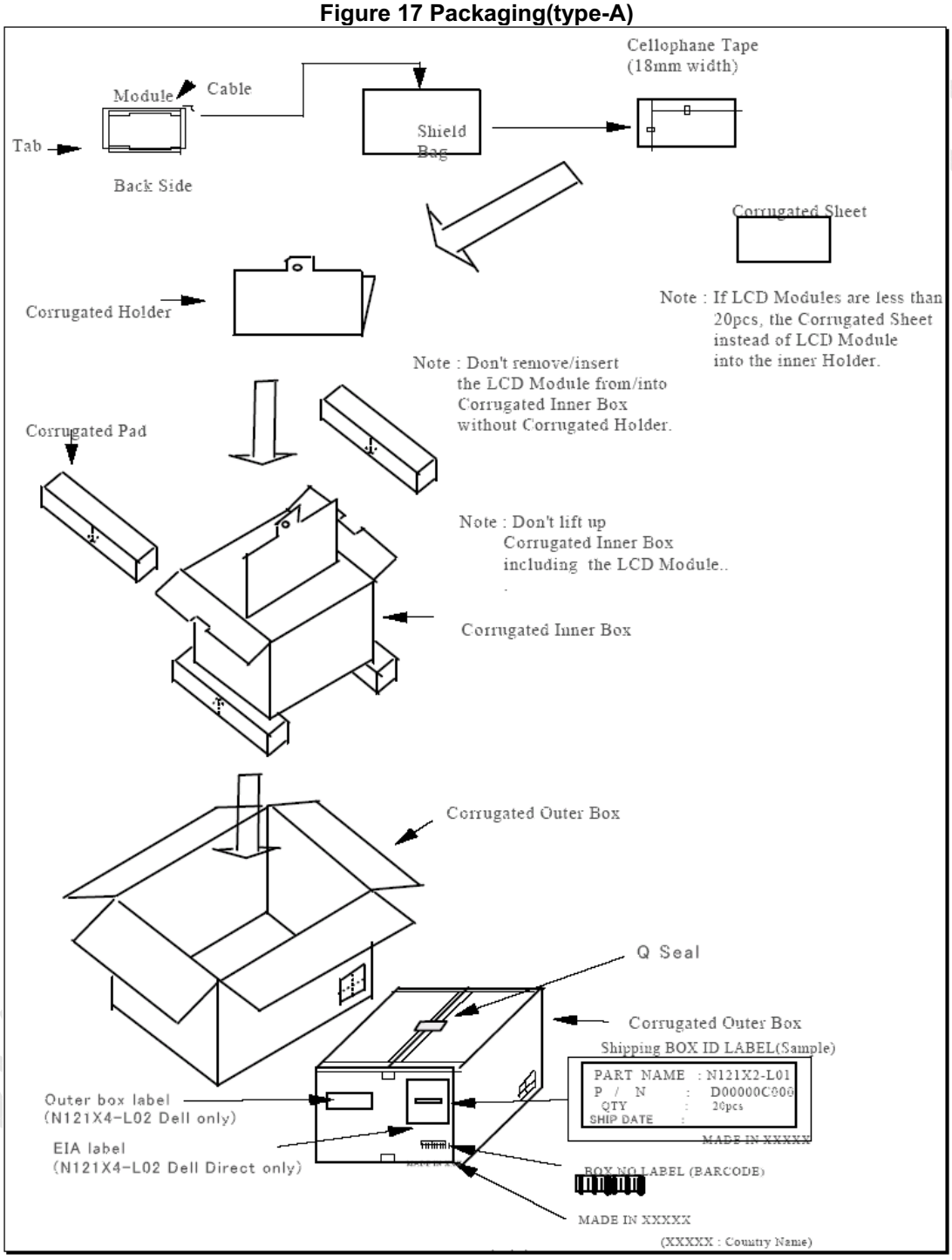
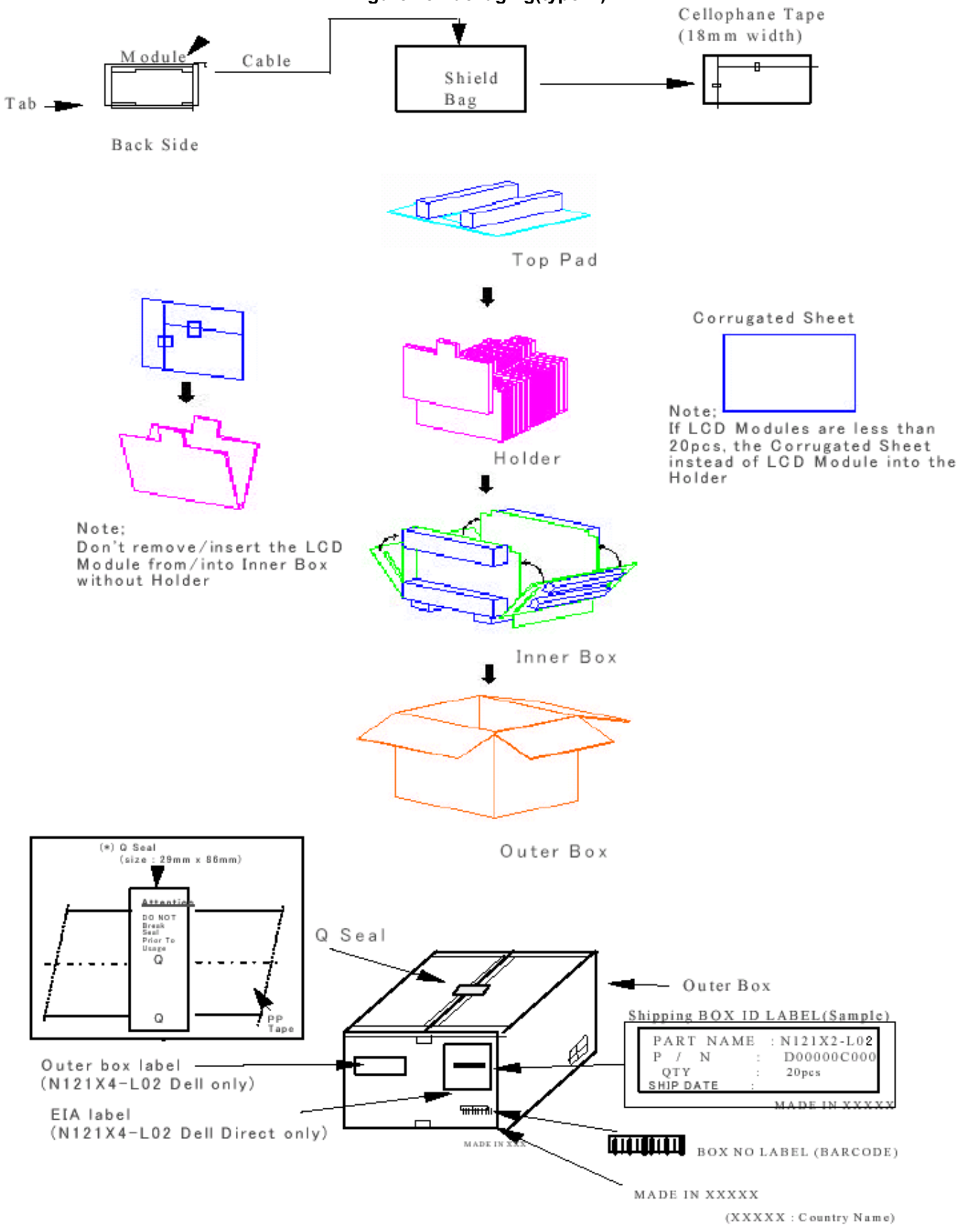


Figure 18 Packaging(type-B)



11. Labels

There are labels on the rear side of the Module.

11.1 Serial Number Label

Figure 19 Serial Number Label

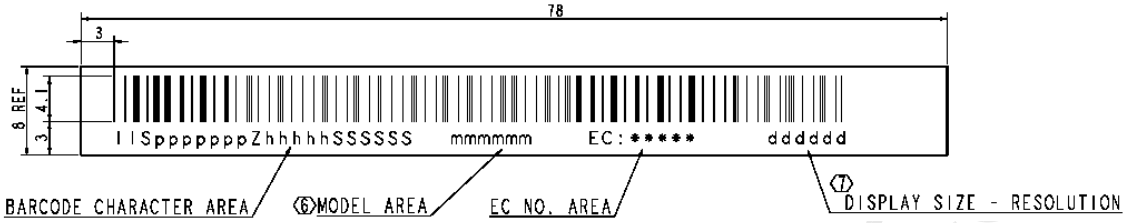
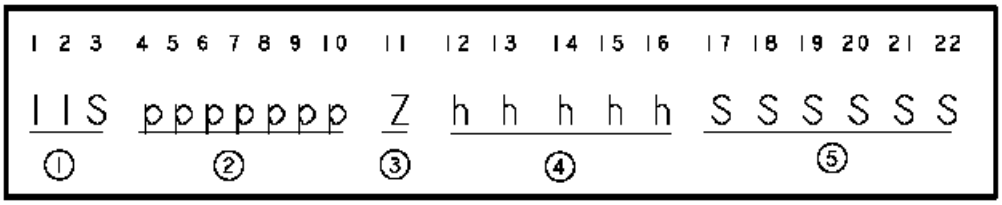


Figure 20 Barcode Character Sequence



① IIS = FIXED
STARTING IDENTIFIER WHICH IS COMMON TO COMPONENT LEVEL SERIAL NUMBERS

② SEVEN DIGIT IDT PART NUMBER ASSIGNED BY THE IDT RELEASING THE PART REFER TO BILL OF MATERIAL.)

③ Z = FIXED
AUTOMATICALLY GIVEN WHEN USING THE IIS-Z FORMAT

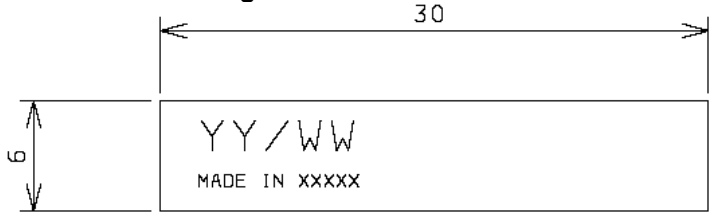
④ hhhhh=HEADER CODE(EC LEVEL) REFER TO BILL OF MATERIAL

⑤ SSSSS=SEQUENCE

11.2 Date Label

YY and WW of the Week Code stand for the Year and the Week of the Year of manufacturing of the Module respectively.

Figure 21 Date label



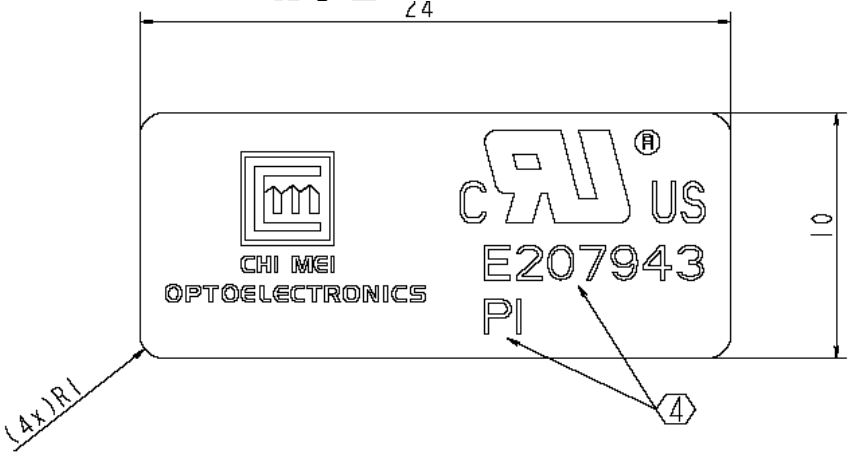
11.3 PPID Label

Figure 22 PPID label

1 CHARACTER COLOR TO BE BLACK.
BACKGROUND COLOR TO BE WHITE.
2 ADHESSIVE TO BE APPLIED ON FAR SIDE.
③FIVE NUMERIC CHARACTERS "SUPID" TO BE APPLIED AS BELOW
PIMES: 46880
FUNAI: 46881
ITP: 46882
4 PRINTED INFORMATION TO COMPLY WITH
DELL SUPPLIER LABELING SPECIFICATION.
⑤TWO NUMERIC CHARACTERS "CO" TO BE APPLIED AS BELOW
PIMES: PH
FUNAI: JP
ITO: CN

11.4 UL Label

Figure 23 UL Label



12. Appendix

12.1 National Test Lab Requirement

The display module will satisfy all requirements for compliance to *UL 60950, 3rd Edition. U.S.A. Information Technology Equipment.*

12.2 Conditions of Acceptability

When installed on the end product, consideration shall be given to the following.

- This component has been judged on the basis of the required specification in *The Standard for Safety of Information Technology Equipment*, CAN/CSA C22.2 No.60950-00 *UL60950, Third Edition, which would cover the component itself if submitted for listing.
- The inverter output circuit is Limited Current Circuits.
- The unit is intended to be supply by SELV and Limited Power Source. Also separated from electrical parts, which may produce high temperature that could cause ignition by as least 13mm of air or by a solid barrio of material of V-1 minimum.
- The terminals and connectors are suitable for factory wiring only.
- A suitable electrical enclosure shall be provided.